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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WEST, JEFFREY R	

ART UNIT	PAPER NUMBER
2857	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/643,193	BHAVNAGARWALA ET AL.	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-13,15-19,26,27,29 and 32-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-13,15-19,26,27,29 and 32-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 October 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1, 3-13, 15-19, 26, 27, 29, and 32-38 are considered to be non-statutory because the claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." State Street, 149 F.3d at 1373, 47 USPQ2d at 1601-02. The purpose of this requirement is to limit patent protection to inventions that possess a certain level of "real world" value, as opposed to subject matter that represents nothing more than an idea or concept, or is simply a starting point for future investigation or research (Brenner v. Manson, 383 U.S. 519, 528-36, 148 USPQ 689, 693-96); In re Ziegler, 992, F.2d 1197, 1200-03, 26 USPQ2d 1600, 1603-06 (Fed. Cir. 1993)).

Furthermore, a process that consists solely of the manipulation of an abstract idea is not concrete or tangible. See In re Warmerdam, 33 F.3d 1354, 1360, 31 USPQ2d 1754, 1759 (Fed. Cir. 1994). See also Schrader, 22 F.3d at 295, 30 USPQ2d at 1459.

Independent claim 1, and dependent claims 3-9, provides a concluding step of "processing the DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices." This final step of "processing" does not produce a "useful, concrete and tangible result" but is instead a result of internal data manipulation that is not externally conveyed. Also, since the resulting processing is not used for any intended purpose, it appears to be only a starting point for future application. For these reasons, claims 1 and 3-9 are considered to be non-statutory.

Independent claim 10, and dependent claims 11-13 and 15-19, similarly provides a concluding step of "characterizing random variations of the integrated circuit using one or more determined Vt variations of transistors of the integrated circuit." This final step of "characterizing" does not produce a "useful, concrete and tangible result" but is instead a result of internal data manipulation that is not externally conveyed. Also, since the resulting characterization is not used for any intended purpose, it appears to be only a starting point for future application. For these reasons, claims 10-13 and 15-19 are considered to be non-statutory.

Claims 26 and 27 present a program storage device embodying a program of instructions. It has been held that, apart from the utility requirement of 35 U.S.C.

101, usefulness under the patent eligibility standard requires significant functionality to be present to satisfy the useful result aspect of the practical application requirement (See Arrhythmia, 958 F.2d at 1057, 22 USPQ2d at 1036). Merely claiming nonfunctional descriptive material stored in a computer-readable medium does not make the invention eligible for patenting. For example, a claim directed to a word processing file stored on a disk may satisfy the utility requirement of 35 U.S.C. 101 since the information stored may have some "real world" value. However, the mere fact that the claim may satisfy the utility requirement of 35 U.S.C. 101 does not mean that a useful result is achieved under the practical application requirement. The claimed invention as a whole must produce a "useful, concrete and tangible" result to have a practical application. In the instant case, similar to claims 1 and 10 described above, independent claims 26 and 27, as well as dependent claims 29 and 32-38, result in final steps of "processing the DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices" and "characterizing random variations of the integrated circuit using one or more determined Vt variations of transistors of the integrated circuit" which are not considered to be "useful, concrete, and tangible" results since they are results of internal data manipulation that are not externally conveyed to carry out an intended purpose.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3, 5-10, 12, 26, 27, 29, and 32, as may best be understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,275,094 to Cranford, Jr. et al. in view of Conti et al., "Test structure for mismatch characterization of MOS transistors in subthreshold regime".

With respect to claim 1, Cranford, Jr. discloses a method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices (column 7, lines 4-9) wherein the DC voltage characteristic data comprises an output DC voltage (column 7, lines 7-9 and column 8, lines 1-4) as a function of an input DC voltage (column 7, lines 14-16) wherein the input voltage is applied to a gate of at least one of the first and second semiconductor transistors (column 7, lines 14-16) and wherein the output voltage is obtained at a common node connection of the first and second semiconductor transistor devices (column 7, lines 7-9) and processing the DC voltage characteristic data to determine a distribution of device mismatch between the semiconductor devices (column 7, lines 20-23 and 28-36).

With respect to claims 3 and 29, Cranford, Jr. discloses that the distribution of device mismatch comprises a distribution threshold voltage mismatch (column 7, lines 28-36).

With respect to claims 6, 12, and 32, Cranford, Jr. discloses that the step of obtaining DC voltage characteristic data for the device pair comprises separately measuring DC voltage characteristic data for each of a plurality of similar device pairs (i.e. either p-type pairs or n-type pairs) (column 7, lines 4-9).

With respect to claim 7, Cranford, Jr. discloses determining a variation in a device characteristic for a device of the integrated circuit comprising the device pair (column 1, lines 6-20 and column 4, lines 9-20).

With respect to claim 8, Cranford, Jr. discloses accessing random variation of device mismatch of the semiconductor integrated circuit (column 1, lines 6-20 and column 4, lines 9-20) using variations in the device characteristic for each device of the integrated circuit (i.e. each pair) (column 7, lines 4-9) as determined from distributions of variation of device mismatch for device pairs within the integrated circuit (column 7, lines 20-23 and 28-36).

With respect to claim 9, Cranford, Jr. discloses that the device characteristic comprises threshold voltage (column 7, lines 28-36).

With respect to claim 10, Cranford, Jr. discloses a method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of obtaining DC voltage characteristic data (column 7, lines 7-9 and column 8, lines 1-4) for one or more selected device pairs of an integrated circuit, wherein the device pairs comprise pairs of neighboring first and second transistors (column 7, lines 4-9) in the integrated circuits (column 1, lines 6-20 and column 4, lines 9-20) wherein the DC voltage characteristic data for a selected device pair comprises an output DC

voltage (column 7, lines 7-9 and column 8, lines 1-4) as a function of an input DC voltage (column 7, lines 14-16) wherein the input voltage is applied to a gate of at least one of the first and second transistors (column 7, lines 14-16) and wherein the output voltage is obtained at a common node connection of the first and second transistors (column 7, lines 7-9) and determining a distribution of threshold voltage mismatch for the a selected device pair using corresponding DC voltage characteristic data for the selected device pair (column 7, lines 20-23 and 28-36), determining a threshold variation of transistors in the integrated circuit using one or more determined distributions of threshold voltage mismatch for selected device pairs (column 1, lines 6-10 and column 7, lines 20-23 and 28-36), and characterizing random variations of the integrated circuit using one or more determined threshold variations of transistors of the integrated circuit (column 1, lines 6-20, column 4, lines 9-20 and column 7, lines 20-23 and 28-36).

With respect to claims 26 and 27, Cranford, Jr. discloses implementing the method using a program storage device readable by a machine tangibly embodying a program of instructions (column 7, lines 26-28).

Cranford, Jr. further discloses that the threshold voltage mismatch between the first and second transistors is when the first and second transistors each comprise an NFET (column 7, lines 4-9).

As noted above, the invention of Cranford, Jr. teaches many of the features of the claimed invention and while Cranford, Jr. does teach obtaining DC voltage

characteristic of a transistor pair, Cranford, Jr. does not explicitly state that the transistors are operating in a subthreshold region.

Conti teaches a test structure for threshold voltage mismatch comprising obtaining subthreshold DC voltage characteristic data for adjacent transistor devices (page 173, column 1, "Introduction, lines 1-9 and page 173, column 2, "Mismatch Model", lines 9-13) by biasing the transistors in a subthreshold region through application of corresponding gate voltages (page 173, "Test Circuits" and page 174, column 1, lines 1-7).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. to include obtaining the DC voltage characteristic for a transistor pair operating in a subthreshold region, as taught by Conti, because, as suggested by Conti, the combination would have improved the analysis and control of mismatch by providing a better estimate of threshold mismatch (page 173, column 1, Introduction, lines 7-9 and page 174, column 1, lines 1-7).

6. Claim 4, as may best be understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. in view of Conti and in view of U.S. Patent No. 6,731,916 to Haruyama.

As noted above, the invention of Cranford, Jr. and Conti teaches many of the features of the claimed invention and while the invention of Cranford, Jr. and Conti does obtain DC voltage characteristic data for a pair of transistors, the combination does not specify retrieving this data from a database.

Haruyama teaches a power amplifying apparatus for a mobile phone including an FET with a bias current setting circuit (column 3, lines 9-11) and a memory/database (column 3, lines 11-13) wherein voltage characteristic data for the FET is stored in the memory/database (column 3, lines 14-20) and, when needed, is retrieved from the memory/database (column 3, lines 42-47).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. and Conti to include retrieving the DC voltage characteristic data from a database, as taught by Haruyama, because the invention of Cranford, Jr. and Conti does teach storing the DC voltage data in a look-up table and Haruyama suggests that the combination would have saved time and effort by storing the characteristic data in a database (column 3, lines 14-20 and column 3, lines 42-47) thereby not requiring the process of measuring the characteristic data each time the mismatch is to be determined in the invention of Cranford, Jr. and Conti.

7. Claims 13 and 33, as may best be understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. in view of Conti et al. and further in view of U.S. Patent No. 5,999,043 to Zhang et al.

As noted above, the invention of Cranford, Jr. and Conti teaches many of the features of the claimed invention and while the invention of Cranford, Jr. and Conti does teach maintaining the transistor pair in a subthreshold region, the combination

does not explicitly describe varying the gate voltages of the transistors to obtain such subthreshold operation.

Zhang teaches an on-chip high resistance device for passive low pass filters with programmable poles comprising a transistor device that is controlled to operate in a subthreshold region through variation in the voltage applied to the gate (column 3, lines 46-49).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. and Conti to explicitly describe varying the gate voltages of the transistors to obtain such subthreshold operation, as taught by Zhang, because the combination of Cranford, Jr. and Conti does teach maintaining the transistor pair in a subthreshold region and Zhang suggests a corresponding method for controlling the transistors to maintain such subthreshold operation, as needed in the invention of Cranford, Jr. and Conti, to obtain accurate threshold voltage mismatch measurements (column 3, lines 46-49).

8. Claims 11 and 34, as may best be understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. in view of Conti et al. and Zhang et al. and further in view of U.S. Patent No. 6,819,183 to Zhou et al.

As noted above, Cranford, Jr. in combination with Conti and Zhang teaches many of the features of the claimed invention and while the invention of Cranford, Jr., Conti, and Zhang does teach maintaining the transistor pair in a subthreshold region by varying gate voltages as needed, the combination does not explicitly

describe keeping the gate voltages of the transistors constant to obtain such subthreshold operation.

Zhou teaches temperature and process compensation of MOSFETs operating in sub-threshold mode wherein a level of a current source is set to maintain a gate voltage of the MOSFET at a constant below its threshold voltage, thereby maintaining operation in a subthreshold region (column 6, lines 17-21).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr., Conti, and Zhang to explicitly describe keeping the gate voltages of the transistors constant to obtain such subthreshold operation, as taught by Zhang, because the combination of Cranford, Jr., Conti, and Zhang does teach maintaining the transistor pair in a subthreshold region by varying gate voltages as needed and Zhang suggests another method for controlling the transistors to maintain such subthreshold operation, as needed in the invention of Cranford, Jr., Conti, and Zhang, when the devices are already operating in a subthreshold region and do not require any variation to obtain accurate threshold voltage mismatch measurements (column 6, lines 17-21).

9. Claims 15, 16, 35, and 36, as may best be understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. in view of Conti et al. and further in view of U.S. Patent No. 4,851,768 to Yoshizawa et al.

As noted above, the invention of Cranford, Jr. and Conti teaches many of the features of the claimed invention, and while the invention of Cranford, Jr. and Conti

does teach determining a distribution of threshold voltage mismatch as a function of input and output voltages in a look-up table (Cranford, Jr.; column 7, lines 20-23 and 28-36), the combination does not explicitly indicate whether a distribution of input voltages is given for a particular output voltage.

Yoshizawa teaches a characteristic test apparatus for an electronic device comprising a transistor pair configured with a node for measuring an output voltage, that varies as a function of the input voltage, between the first and second transistors (Figure 2a) wherein a varying/distribution of input voltages are applied to obtain voltage output to determine a threshold voltage as part of a DC voltage characteristic (column 4, lines 59-67) wherein the threshold voltage can be determined either by determining the distribution of input voltages for a given output voltage or determining a distribution of output voltages for a given input (column 6, lines 6-17).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. and Conti to explicitly include a distribution of input voltages for a particular output voltage, as taught by Yoshizawa, because the invention of Cranford, Jr. and Conti does provide a distribution of threshold voltage mismatch as a function of input and output voltages in a look-up table and Yoshizawa suggests a corresponding method for determining such a distribution that would have aided the user by implementing known relationships between input/output voltage and threshold mismatch to allow the user to determine threshold voltage mismatches as part of the look-up table using either known input voltage

levels or known output voltage levels as available (column 4, lines 59-67 and column 6, lines 6-17).

10. Claim 18, as may best be understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. in view of Conti and further in view of U.S. Patent No. 6,181,621 to Lovett.

As noted above, the invention of Cranford, Jr. and Conti teaches many of the features of the claimed invention and while the invention of Cranford, Jr. and Conti does teach characterizing mismatch in a semiconductor integrated circuit, the combination does not specify that the integrated circuit be an SRAM.

Lovett teaches a threshold voltage mismatch compensated sense amplifier for SRAM memory arrays comprising means for obtaining threshold voltage mismatch information in a SRAM (column 1, lines 6-10 and column 2, lines 7-15).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. and Conti to specify that the integrated circuit be an SRAM, as taught by Lovett, because the invention of Cranford, Jr. and Conti does teach employing a threshold voltage mismatch compensated sense amplifier (Cranford, Jr.; column 7, lines 4-5 and 20-23) and Lovett suggests that SRAM devices are devices that employ compensated sense amplifiers (column 1, lines 6-10) and are greatly affected by threshold mismatches due the size constraints of such SRAMs (column 3, line 65 to column 4, line 7) and therefore the combination would have

provided greater utility in the invention of Cranford, Jr. and Conti by applying the method to the SRAM devices.

Further, it has been held that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). In the instant case the structure of Cranford, Jr. and Conti is capable of characterizing transistor mismatch in any of a wide variety of integrated circuits, such as an SRAM, and therefore meets the claim.

11. Claims 19 and 38, as may best be understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cranford, Jr. et al. in view of Conti et al. and further in view of U.S. Patent No. 6,798,278 to Ueda.

As noted above, the invention of Cranford, Jr. and Conti teaches many of the features of the claimed invention and while the invention of Cranford, Jr. and Conti does teach a determining a voltage threshold variation of transistors in an integrated circuit using a microprocessor measuring an output voltage as a function of an input voltage, the combination does not specifically indicate determining the variation by determining a standard deviation of threshold voltage variation of the transistors.

Ueda teaches a voltage reference generation circuit and power source incorporating such a circuit wherein a variation in threshold voltage mismatch is

determined for a transistor pair by determining a standard deviation (column 13, lines 28-41).

It would have been obvious to one having ordinary skill in the art to modify the invention of Cranford, Jr. and Conti to specifically determine a standard deviation of threshold voltage variation of the transistors, as taught by Ueda, because the invention of Cranford, Jr. and Conti does teach determining threshold voltage mismatch indicating the similarity of the transistors using a processor that corrects for the voltage mismatch and Ueda suggests a corresponding conventional method for determining such variation that would have expressed the variation in terms of a standard deviation that is comparable to accepted limits, thereby increasing the efficiency of the invention of Cranford, Jr. and Conti, by allowing the processor to determine when the variation is outside such limits and the correction needs to be performed (column 13, lines 28-41).

Response to Arguments

12. Applicant's arguments filed 26 October 2006 have been fully considered but they are not persuasive.

With respect to the outstanding 35 U.S.C. 101, rejection, Applicant argues:

> The Examiner's rejection of claims 1 and 10 are erroneous. One fundamental flaw in the 101 rejections is that the Examiner fails to consider the claim language of claims 1 and 10 in the entirety. On a general level, claims 1 and 10 are directed to methods for characterizing device mismatch in a semiconductor integrated circuit by obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices, wherein the DC voltage characteristic data comprises an output DC voltage VOUT as a function of an input DC voltage VIN, and using the DC voltage characteristic data to

determine a distribution of device mismatch between the first and second semiconductor transistor devices.

In formulating the rejection of claims 1 and 10, the Examiner only considers the "final step of processing" of claim 1 and the "final step of characterizing" in claim 10, contending that such steps do not produce a useful concrete and tangible result but is instead a result of internal data manipulation that is not externally conveyed. This analysis is legally erroneous on its face as the Examiner fails to consider the claimed invention as a whole. Indeed, with regard to claims 1 and 10, the Examiner's has not fairly explained how the claimed inventions, as a whole, are not limited to practical applications within the technological arts.

In any event, when the claims are properly construed in view of Applicants' specification and in the perspective of one of ordinary skill in the art, it should be readily clear that the claimed inventions are directed to processes that undoubtedly produce a concrete tangible result of characterizing device mismatch of transistor pairs in an integrated circuit using DC voltage.

With regard to claims 26 and 27, the above arguments equally apply. Furthermore in addressing claims 26 and 27, the Examiner fails to consider that the claimed inventions of claims 26 and 27 are directed to a program storage device readable by a machine, tangible embodying a program of instructions executable by the machine to perform method steps for characterizing device mismatch in a semiconductor integrated circuit. In this regard, the Examiner's analysis and findings are not on point as the claimed inventions are directed NOT to a process, per se, but rather a device - a program storage device having instructions for performing the claimed process steps.

As explained in MPEP 2106(IV)(B)(1), descriptive material can be characterized as either "functional descriptive material" or "nonfunctional descriptive material." In this context, "functional descriptive material" consists of data structures and computer programs which, impart functionality when employed as a computer component. When functional descriptive material is recorded on some computer-readable medium it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized. Here, at the very least, claims 26 and 27 are properly viewed as being directed to program storage devices having functional description material recorded thereon, and are thus, directed to statutory subject matter.

The Examiner maintains that, as set forth in the August 2006 revision of the MPEP, a claimed invention is directed to a practical application of a 35 U.S.C. 101

judicial exception when it: "transforms" an article or physical object to a different state or thing; or otherwise produces a useful, concrete and tangible result.

In the instant case, claims 1 and 10 do not provide a transformation or reduction of an article to a different state or thing, but instead only obtain and processes voltage characteristic data with this obtaining and processing of voltage characteristic data performing no physical transformation but instead providing data manipulation.

In the instant case, claims 1 and 10 also do not provide a useful, concrete and tangible result, but instead result in a concluding step of "processing the DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices" and "characterizing random variations of the integrated circuit using one or more determined Vt variations of transistors of the integrated circuit". These final steps of "processing" and "characterizing" do not produce a "useful, concrete and tangible result" but are instead a result of internal data manipulation that is not externally conveyed, specifically the method does not output, store, or produce any tangible form of the processing/characterizing to accomplish a practical application.

The Examiner maintains that in determining whether the claim is for a "practical application," the focus is not on whether the steps taken to achieve a particular result are useful, tangible and concrete, but rather that the final result is "useful, tangible and concrete."

With respect to claims 26 and 27, the Examiner agrees that a claimed computer-readable medium encoded with a data structure defines structural and functional interrelationships between the data structure and the computer software and hardware components which permit the data structure's functionality to be realized, and thus can be statutory.

The Examiner also asserts, however, that it has been held that, apart from the utility requirement of 35 U.S.C. 101, usefulness under the patent eligibility standard requires significant functionality to be present to satisfy the useful result aspect of the practical application requirement (See Arrhythmia, 958 F.2d at 1057, 22 USPQ2d at 1036). Merely claiming nonfunctional descriptive material stored in a computer-readable medium does not make the invention eligible for patenting. For example, a claim directed to a word processing file stored on a disk may satisfy the utility requirement of 35 U.S.C. 101 since the information stored may have some "real world" value. However, the mere fact that the claim may satisfy the utility requirement of 35 U.S.C. 101 does not mean that a useful result is achieved under the practical application requirement. The claimed invention as a whole must produce a "useful, concrete and tangible" result to have a practical application. In the instant case, similar to claims 1 and 10 described above, independent claims 26 and 27, as well as dependent claims 29 and 32-38, result in final steps of "processing the DC voltage characteristic data to determine a distribution of device mismatch between the first and second semiconductor transistor devices" and "characterizing random variations of the integrated circuit using one or more

determined Vt variations of transistors of the integrated circuit" which are not considered to be "useful, concrete, and tangible" results since they are results of internal data manipulation that are not externally conveyed to carry out an intended purpose.

Regarding the outstanding 35 U.S.C. 103(a) rejections, Applicant argues:

> Out the outset, it appears that the Crux of the rejections is seemingly based on the Examiners misunderstanding, or outright lack of understanding, of the claimed subject matter. Indeed, this is evidenced by each claim rejection being preceded by "as may best be understood", as well as the continued misunderstanding as to the difference between DC current and DC voltage. If the Examiner is having difficulty in understanding the subject matter of the claimed inventions, it is requested that the Examiner contact the undersigned attorney for clarification.
>
> In general, the crux of the rejections is based on clear misinterpretations and mischaracterizations of the teachings of Cranford and Conti as applied to the claimed inventions. For example, the Examiner's reliance on the unrelated teachings of Cranford is bewildering as Cranford is directed to a method for dynamically adjusting the threshold voltage of a CMOS device in a receiver to provide improved noise margin and to a method for dynamically matching the threshold voltages in a differential amplifier to correct for manufacturing offset (See Abstract).

The Examiner first asserts that the rejection of the claims is indicated as "as may best be understood" since the rejection is of non-statutory claims.

With respect to Applicant's argument that Cranford is unrelated because it is "directed to a method for dynamically adjusting the threshold voltage of a CMOS device in a receiver to provide improved noise margin and to a method for dynamically matching the threshold voltages in a differential amplifier to correct for manufacturing offset", the Examiner asserts that Applicant's invention is of "circuits

and methods for measuring and characterizing device mismatch of semiconductor transistors due to local variations in device characteristics resulting from random sources, and in particular, Vt (threshold voltage) variations between neighboring MOSFETs..." Therefore, since Cranford is for "dynamically adjusting a threshold voltage of a CMOS...and to a method for dynamically matching the threshold voltages" and Applicant's invention is for "characterizing device mismatch of semiconductor transistors...in particular Vt (threshold voltage) variations between neighboring MOSFETs", the invention of Cranford is quite related to the instant invention since they both deal with threshold voltage mismatch and one having ordinary skill in the art would recognize that in order to dynamically adjust a mismatched threshold voltage, the mismatch must first be characterized.

Applicant then argues:

> The Examiner's attempt to explain the rejection of claim 1 (Office Action, page 18, et seq.) with regard to Cranford is unclear and glaringly fails to consider the claim language. For instance, the Examiner contends, without support, that Cranford in Col. 8, lines 1-4, in conjunction with FIG. 8 clearly describes that the output voltage obtained from the common node connection between the first and second transistor devices comprises a DC voltage corresponding to device mismatch. However, Col. 8, lines 1-4 of Cranford states that:
>
> > FIG. 8 shows the change in various harmonics in the output signal 163 after the offset voltage supplied by the feedback circuit 150 is provided to the transistors connected to the output terminal 116, 120 (see FIG. 5)
>
> The Examiner does not explain how this is even remotely related to the invention of claim 1. Indeed, at the very least, the Examiner fails to address the claim language of claim 1 which recites, in part, obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices, wherein the DC voltage characteristic data comprises an output DC voltage VOUT a function of an input DC voltage VIN, wherein VIN is

applied to a gate of at least one of the first and second semiconductor transistor devices and wherein VOUT is obtained at a common node connection of the first and second semiconductor transistor devices...Notwithstanding the lack of explanation, FIG. 8 is nothing more that a representation of the offset in FIG. 7 in terms of amplitude and frequency for the various harmonics in the output signal prior to correction of offset voltage (see, Col, 5, lines 4.-6). In other words, FIG, 8 illustrates Amplitude (in db) of the output signal as a function of Frequency (i.e.. Output Voltage Amplitude vs. Frequency).

In stark contrast, as clearly recited in the claimed inventions, the DC voltage characteristic data for a device pair comprises an output DC voltage VOUT as a function of an input DC voltage VIN. In this regard, the Examiner cannot reasonably argue that FIG. 8 Cranford discloses DC voltage VOUT as a function of an input DC voltage VIN especially given the clear explicit teachings of Cranford as to what FIG. 8 represents. In this regard, the Examiner's arguments as premised on Cranford are fundamentally flawed on both technical and legal grounds.

The Examiner asserts that the previous Office Action indicated that, with respect to claim 1, Cranford, Jr. discloses a method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices (column 7, lines 4-9) wherein the DC voltage characteristic data comprises an output DC voltage (column 7, lines 7-9 and column 8, lines 1-4) as a function of an input DC voltage (column 7, lines 14-16) wherein the input voltage is applied to a gate of at least one of the first and second semiconductor transistors (column 7, lines 14-16) and wherein the output voltage is obtained at a common node connection of the first and second semiconductor transistor devices (column 7, lines 7-9) and processing the DC voltage characteristic data to determine a distribution of device mismatch between the semiconductor devices (column 7, lines 20-23 and 28-36).

These cited sections of Cranford, Jr. disclose:

> Turning to FIG. 4, a differential amplifier 100 incorporating CMOS transistors 102 and 104 (shown in FIGS. 1A and C) have p type devices 7, 25 coupled to n type devices 29, 28 through their common drain electrodes. An output circuit 118 is coupled to the common drain electrodes 116, 120. (column 7, lines 4-9)
>
> The n type devices 29, 28 gate electrodes are connected to an input positive signal 114 and an input minus signal 112, respectively. (column 7, lines 14-16)
>
> FIG. 5 shows one example of a voltage feedback circuit 150 which automatically generates a voltage for correction of the threshold mismatch between n type device 28 and 29 as a result of manufacture. (column 7, lines 20-23)
>
> The Fast Fourier Transforms (FFT) application is executed for detection of harmonic differences between the signals at the input and output terminals and introduced by threshold offset which is a well-known technique. Based on the harmonic differences identified by the FFT in the input-output signals and indicative of the offset between the n type devices 29, 28, the table 156 can be constructed to indicate a voltage level to correct the offset. (column 7, lines 28-36)
>
> FIG. 8 shows the change in the various harmonics in the output signal 163 after the offset voltage supplied by the feedback circuit 150 is provided to the transistors connected to the output terminals 116, 120 (See FIG. 5). (column 8, lines 1-4)

Therefore, the Examiner maintains that Cranford, Jr. discloses a device pair comprising first and second semiconductor transistor devices (i.e. nFETs N28 and N29), obtaining DC voltage characteristic data for the device pair (i.e. input and output signals obtained by the microprocessor as part of the voltage feedback circuit) wherein the DC voltage characteristic data comprises an output DC voltage VOUT a function of an input DC voltage VIN (i.e. the DC offset voltage measured in the voltage feedback circuit as a function of the input voltage applied to the transistors), wherein VIN is applied to a gate of at least one of the first and second

semiconductor transistor devices (i.e. inputs 112/114 applied to nFET gate) and wherein VOUT is obtained at a common node connection of the first and second semiconductor transistor device (i.e. common outputs 116/120).

The Examiner maintains that the description of Figure 8 describes that the DC offset voltage of the voltage amplitude of the semiconductor transistor pair has been correctly compensated. This compensation is the threshold voltage mismatch that has been determined from the obtained VIN and VOUT and therefore, since one having ordinary skill in the art would recognize that in order to determine DC voltage offset between two transistor devices, the DC voltage offset must first be measured, this description, in combination with the other cited sections of Cranford, Jr., does disclose DC voltage VOUT as a function of an input DC voltage VIN.

Applicant then argues:

> Moreover, it could not be any more clear that the Examiner's reliance on Conti in support of the claim rejections is grossly misplaced as Conti teaches a mismatch model based on measurements of drain current ID (see page 173, second column on bottom). The Examiner continues to misunderstand the fundamental difference between DC Voltage characteristic data (as claimed) and DC Current characteristic data (as disclosed in Conti). The Examiner should review pages 6-9 of the Background section of Applicants' specification, which explains the problems associated with the use of DC current characteristic data for purposes of evaluating device mismatch.

The Examiner asserts that the invention of Conti specifically indicates that "mismatch characterization of MOS transistor operating in subthreshold regime becomes extremely important for an accurate design" (page 173, column 1, Introduction, lines 7-9) and "estimation of ΔV_{TH} is more accurate in subthreshold

rather than in saturation regime, since the effect on I_D or a variation of V_{TH} is more pronounced as can be seen..." (page 174, column 1, lines 1-7).

The Examiner asserts that since Crawford teaches obtaining the DC output voltage characteristic data from a common node terminal connecting the transistor pair drain terminals (Crawford; column 7, lines 7-9) and since it is well known that the output voltage is directly proportional to the output current, Conti suggests that operating the transistors in the subthreshold region would have provided more pronounced mismatch determination in the voltage characteristic of Crawford.

Therefore, the Examiner's reliance upon Conti is not for any measurements of drain current. Instead, the Examiner is relying on a teaching that that operating transistors in the subthreshold region provides more pronounced mismatch determination. Since output voltage is directly proportional to output current, this more pronounced mismatch occurs when drain voltage is measured as well and therefore is applicable to the invention of Cranford.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

U.S. Patent Application Publication No. 2004/0193390 to Drennan et al. teaches a method and apparatus for rapid evaluation of component mismatch in integrated circuit performance.

U.S. Patent No. 5,598,115 to Holst teaches a comparator cell for use in a content addressable memory comprising a transistor pair providing a match sense output.

U.S. Patent No. 6,628,146 to Tam teaches a comparator circuit and method that determines a distribution of Vin for Vout of a transistor pair.

U.S. Patent No. 6,161,213 to Lofstrom teaches a system for providing an integrated circuit with a unique identification by plotting a distribution of threshold voltage mismatch between pairs of MOSFETs.

Bastos et al., "Mismatch characterization of small size MOS transistors" teaches a method for characterizing device mismatch in a semiconductor integrated circuit.

Shen et al., "Down Literal Circuit with Neuron-MOS Transistors and Its Applications" teaches a method for determining PMOS and NMOS threshold voltages and corresponding mismatch based on measured Vout vs Vin characteristics.

Lakshmikumar et al., "Characterization and Modeling of Mismatch in MOS Transistors for Precision Analog Design" teaches the determination of physical causes of mismatch for both p and n-channel devices.

Pavasovic et al., "Characterization of Subthreshold MOS Mismatch in Transistors for VLSI Systems" teaches the determination of subthreshold mismatch in transistor pairs.

Bhavnagarwala et al., "The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability" teaches the determination of threshold voltage distribution functions for SRAM devices.

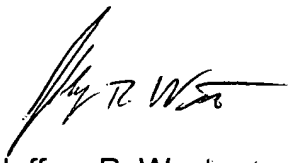
14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (571)272-2226. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571)272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jeffrey R. West
Examiner – AU 2857

January 6, 2007